Input matching with a physical resistor

Input matching could be done with a physical 50Ω resistor. This would be sufficient to avoid most reflections e.g. when connecting a commercial signal generator to a DUT that is of higher input impedance. The typical input capacitance could also be neutralized with a shunt inductor so as to resonate at the wanted frequency. How to compute the noise factor of this circuit? Recall the definition of $F = vn_{O,TOT}^2/vn_{O,RS}^2$ where the first term in the total output noise voltage power spectral density (PSD) and the second the output noise voltage PSD due to Rs, the source resistance. The latter is simply 4kTRs multiplied by the square of the voltage divider gain RL/(Rs+RL).

$$V_{n,O,Rs}^2 = 4kT \cdot R_S \cdot \left(\frac{R_L}{R_S + R_L}\right)^2$$

To compute the total output noise, we apply the superposition principle after shorting all voltage sources and leaving open all current ones except for the one we are considering. RS and RL are thus in parallel each with a 4kTR equivalent noise voltage PSD. We may compute the equivalent output noise voltage PSD in two ways:

1. Place the voltage noise PSD of each resistor near their ground terminal rather than at the Vin node; apply in turn the correct squared voltage gain to compute the equivalent voltage noise density at node Vin; sum the two contributions. The contribution of Rs is exactly as calculated above, but the contribution of RL sees a different voltage divider radio Rs/(Rs+RL)

$$V_{n,O,TOT}^2 = 4kT \cdot R_S \cdot \left(\frac{R_L}{R_S + R_L}\right)^2 + 4kT \cdot R_L \cdot \left(\frac{R_S}{R_S + R_L}\right)^2 = 4kT \cdot \frac{R_S {R_L}^2 + R_L {R_S}^2}{(R_S + R_L)^2}$$
$$= 4kT \cdot \left(\frac{R_S R_L}{R_S + R_L}\right) = 4kT \cdot \left(R_S + R_L \cdot \frac{R_S^2}{R_L^2}\right) \cdot \left(\frac{R_L}{R_S + R_L}\right)^2$$

   The last form of the output noise eliminates the different divider ratio by multiplying the voltage noise PSD of RL by the square of Rs/RL, the equivalent square of the voltage gain needed to transfer the RL noise to Rs and use then the same voltage divider factor

2. Express the resistor noise as a current PSD given by 4kT/R (indeed the power PSD is also 4kT and thus equivalent for both representations); sum the current PSD; convert back to a voltage noise PSD after multiplying by the square of the equivalent resistance

$$V_{n,O,TOT}^2 = 4kT \cdot \left(\frac{1}{R_S} + \frac{1}{R_L}\right) \cdot \left(\frac{R_S R_L}{R_S + R_L}\right)^2 = 4kT \cdot \left(\frac{R_S R_L}{R_S + R_L}\right)$$

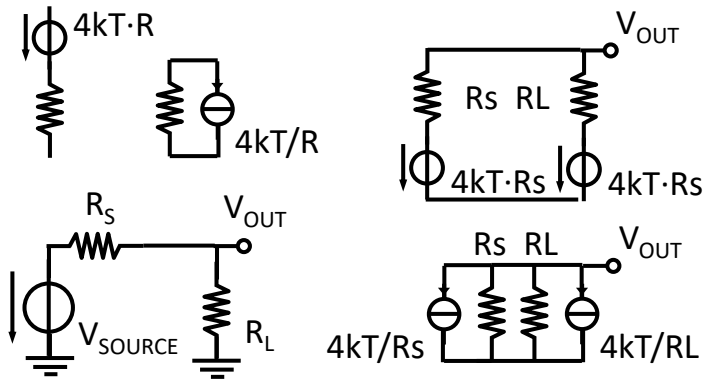


Figure 1. Bottom left : input matching with RL; top left: two equivalent representation for resistor noise as vn^2 [V^2/Hz] or in^2 [A^2/Hz]; top right: equivalent noise circuit according to 1); bottom right: ibid according to 2)

The noise factor is simply given by the ratio of the two computed output voltage PSD

$$F = \frac{V_{n,O,TOT}^2}{V_{n,O,Rs}^2} = \frac{4kT \cdot \left(\frac{1}{R_S} + \frac{1}{R_L}\right) \cdot \left(\frac{R_S \cdot R_L}{R_S + R_L}\right)^2}{4kT \cdot R_S \cdot \left(\frac{R_L}{R_S + R_L}\right)^2} = \frac{4kT \cdot \left(\frac{1}{R_S} + \frac{1}{R_L}\right) \cdot R_S^2 \cdot \left(\frac{R_L}{R_S + R_L}\right)^2}{4kT \cdot R_S \cdot \left(\frac{R_L}{R_S + R_L}\right)^2}$$

$$= \frac{4kT \cdot R_S + \frac{4kT}{R_L} \cdot R_S^2}{4kT \cdot R_S} = 1 + \frac{R_S}{R_L}$$

Note carefully that the numerator expression was chosen as that derived with method 2) before the simplification. Factoring Rs^2 from the squared term of that numerator yields the rightmost expression. One may notice that both the numerator and denominator have now the same squared voltage gain term from Vsource to Vout. Dividing both the numerator and denominator with this gain refers the noise back to the input node Vsource, where we recognize the voltage noise source PSD of Rs added to the current noise PSD of RL (4kT/RL) multiplied by the square of the input resistance Rs to transform it back to a voltage noise PSD. The noise factor could thus as well be defined at the input node after expressing the circuit noise as an equivalent input voltage and current PSD as in our lecture notes copied below.

$$F = \frac{V_{n,S,Rs}^2 + \left(V_{n,\mathrm{in},Circ}^2\right) + R_s^2 \cdot I_{n,\mathrm{in},Circ}^2}{V_{n,S,Rs}^2}$$

Counter-intuitively, the input current noise PSD is only multiplied by the square of Rs without taking into account the circuit input impedance (RL in our study case here). Also note that the circuit input voltage noise PSD is zero in our particular case, thus placed in bracket above, and that we could not use the voltage noise PSD 4kTRL directly instead of its current equivalent representation. It probably works for a voltage noise PSD associated with a high impedance node, such as 1/f noise for a BJT or MOS transistor for which we model the output voltage noise after multiplying it by the square of the transistor gm. It is thus safer to compute noise at the output to derive F. To find the correct results when describing the noise of RL with a voltage noise PSD we must apply the square of the gain (RS/RL) which allows us to transfer the noise from RL to Rs as was illustrated in 1) above. The fact that usually RL=Rs, thus the gain is unity, might be responsible for that error seen in textbooks !

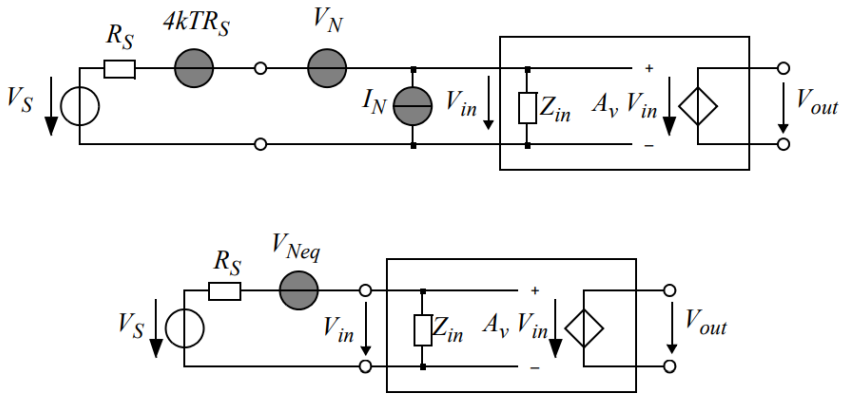


Fig 5-9: *Noisy amplifier and equivalent noise sources.*

The PSD of the output noise is given by:

$$S_{VNout} = |A_v(f)|^2 \left\{ \underbrace{\left|\frac{Z_{in}}{Z_{in}+R_S}\right|^2 S_{VN} + \left|\frac{R_S Z_{in}}{Z_{in}+R_S}\right|^2 S_{IN}}_{\text{contribution of the amplifier}} + \underbrace{\left|\frac{Z_{in}}{Z_{in}+R_S}\right|^2 4kTR_S}_{\text{contribution of the source}} \right\} \tag{5.35}$$

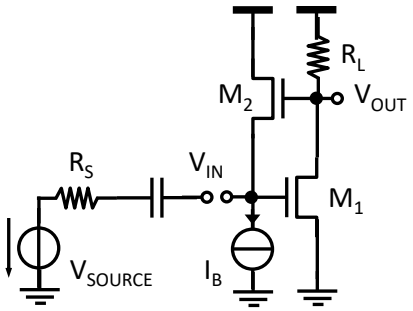
LNA based on a current conveyor

The main goal here is to find a way to impose a well-defined input impedance without the noise associated to a physical resistor leading as we have seen before to a NF of 3dB without providing any RF gain.

An LNA based on a current conveyor is sketched below. It is formed with a gain stage M1 loaded by RL. A feedback path formed with M2 biased with a current source I_B operates as a voltage follower. Let's consider the input node Vin. How is its DC voltage defined? If Vin = 0, M1 is off and Vout = VDD. This leads to a large current in M2 bigger than I_B (by proper design) which charges Vin and start pulling Vout at a lower voltage so that the RL and M1 current are equal. M2 forms thus a negative feedback path setting the DC voltage level Vin so that M1 exactly sinks the RL current. Vin is thus close to M1 threshold voltage depending on its sizing.

Any deviation of Vin, e.g. positive increases the current of M1, lowering Vout thus the current delivered by M2 forcing the circuit to retrieve the equilibrium point. Conversely a negative step on Vin reduces M1 current leading to a Vout raise injecting in turn more current into Vin.

Vout DC voltage is set by M2 since its VGS voltage difference must ensure that M2 exactly delivers I_B. If M2 substrate is at VSS, Vout is close to $VTN_{M1}+n\cdot VTN_{M2}$, n~1.3 being the MOS slope factor. A local bulk connection eliminates the substrate effect. The minimum voltage to operate such a structure is hence $2\cdot VTN+RL\cdot I_{M1}$.



Deriving the Kirchhoff equations

The circuit has two nodes that we call Vin and Vout (Vo in the equations). For each node we may write that the sum of all small signal currents should be 0. We have thus to find the coefficients a, b, c, d of the following matrix:

$$\begin{pmatrix}0\\0\end{pmatrix}=\begin{pmatrix}a & b\\c & d\end{pmatrix}\cdot\begin{pmatrix}V_{IN}\\V_O\end{pmatrix}$$

By definition, a current entering a device is given the positive sign and vice versa.

Let's start with the Vin node.

1. The DC source by virtue of superposition is replaced by an open circuit and vanishes.
2. Neglecting the capacitance of the gate of M1, no current flows towards M1 If we want to model that effect the current is simply given by $s\cdot C_{GS}\cdot$Vin. C_{GD} is much smaller than the former if M1 is saturated (channel is pinched!) but if there is a large voltage gain Vo/Vin, the equivalent capacitance is multiplied by the Miller effect! We could model this with a current $s\cdot C_{GS}\cdot$(Vin-Vo)
3. The small signal current depends however on both Viin and Vo owing to M2. Let's use the convention that a current flowing towards a device is defined as positive while a current

exiting a device is defined as negative. The DC current of M2 depends on the gate (Vo) to source (Vin) voltages. In subthreshold we may write for the drain current if M2 is saturated

$$I_D = IS \cdot e^{\left(\frac{V_G - V_T}{n \cdot U_T} - \frac{V_S}{U_T}\right)}$$

Applying a small perturbation dVG produces a variation of the output current dID. This transconduction dID/dVG is given by the derivative of the above equation.

$$\frac{dI_D}{dV_G} = gm = \frac{1}{n \cdot U_T} \cdot IS \cdot e^{\left(\frac{V_G - V_T}{n \cdot U_T} - \frac{V_S}{U_T}\right)} = \frac{I_D}{n \cdot U_T}$$

Similarly, a variation of VS could be described with

$$\frac{dI_D}{dV_S} = gms = -\frac{1}{U_T} \cdot IS \cdot e^{\left(\frac{V_G - V_T}{n \cdot U_T} - \frac{V_S}{U_T}\right)} = -\frac{I_D}{U_T}$$

Indeed, raising VG increases the current while raising VS reduces the current hence the negative sign. However, let's consider that gms is positive thus simply n times bigger than gm and we shall find the appropriate sign according to the current direction as proposed just above. Thus, from now on we use

$$gms = \frac{I_D}{U_T}$$

The DC current ID flows from the device towards VIN thus is given a negative sign. Raising VIN (VS) reduces that current which we model with a positive current flowing into M2. The net current is thus indeed -ID+dID. Coefficient 'a' is thus simply gms2. Raising Vo increases ID, thus the current variation goes from M2 towards Vin and should thus be given a negative sign. Coefficient b is thus -gm2.

Raising the Vout node, leads to some current flowing through RL hence c is simply 1/RL. Again, the DC current of R2 is negative (exiting the device) hence the current variation is positive. When Vin is raised, M1 current is increased by gm1·dVin hence coefficient d is gm1.

Our two Kirchhoff equations are thus given by

$$\begin{pmatrix} 0 \\ 0 \end{pmatrix} = \begin{pmatrix} g_{ms2} & -g_{m2} \\ g_{m1} & 1/R_L \end{pmatrix} \cdot \begin{pmatrix} V_{IN} \\ V_O \end{pmatrix}$$

It describes how our circuit will react to a perturbation applied on either Vin or Vout. If we force Vin, the variation on Vin is indeed dVin and any current difference is absorbed by the voltage source imposing the perturbation. However, from the second equation we may calculate how Vout is affected.

$$V_O = -g_{m1} \cdot R_L \cdot V_{IN}$$

Indeed, raising Vin increases M1 current , hence the voltage drop across RL should increase via a reduction of Vo (hence the negative voltage gain).

How are gm1 and RL related? In subthreshold gm1=ID/nUT while 1/RL=ID/(VDD-Vout) where ID is M1 drain current which is also flowing through RL. Depending on the VDD level we may increase the voltage drop across RL. It could thus be made much bigger than nUT which is 30mV at 25°C. Consequently, gm1·RL, given by the voltage ratio, could be made >>1 providing voltage gain.

From the upper equation we find how a perturbation on Vo affect Vin,

$$g_{ms2} \cdot V_{IN} = g_{m2} \cdot V_O$$

If M2 has its local bulk connected at node VIN, gms2=gm2 (VG above is indeed referred to the bulk node of the NMOS, which is VSS=0; with a local bulk, VG becomes VGS=VG-VS and VS becomes VS-VS=0), thus we have a pure voltage follower with a gain of unity. In the other case the Vin voltage is attenuated by the body factor n~1.3.

Calculating the input impedance of the circuit

Out set of equations is still valid but now we perturbate our circuit with a current fed in at the input to see how it will react. Kirchhoff states that the sum of all currents should be zero. It is however more convenient to place the current on the opposite side of the equal sign hence we have to swap its sign. Injecting a current towards our node would indeed be considered as a negative one with the sum null. The equation just states slightly differently that all the current that is injected into the circuit could only flow towards other devices hence respecting Kirchhoff laws.

$$\begin{pmatrix} I_{IN} \\ 0 \end{pmatrix} = \begin{pmatrix} g_{ms2} & -g_{m2} \\ g_{m1} & 1/R_L \end{pmatrix} \cdot \begin{pmatrix} V_{IN} \\ V_O \end{pmatrix}$$

To find the circuit input admittance, we should solve the system of equations to eliminate Vo. The second equation allows that calculation, and one obtains

$$Y_{IN} = \frac{I_{IN}}{V_{IN}} = g_{ms2} + g_{m2} \cdot g_{m1} \cdot R_L$$

Now we find the condition for input matching without (first) and with local bulk (second)

$$Z_{IN} = \frac{1}{g_{ms2} + g_{m2} \cdot g_{m1} \cdot R_L} = R_s$$

$$\frac{1}{g_{m2} \cdot (1 + g_{m1} \cdot R_L)} = R_S$$

Interestingly we could move gm2 on the other side of the equality obtaining

$$\frac{1}{(1 + g_{m1} \cdot R_L)} = g_{m2} \cdot R_S$$

The rightmost term should thus be smaller than unity. Indeed, recalling that gm1·RL is the circuit voltage gain, this gives us meaningful circuit design guidelines. A voltage gain of 9 (19dB) yields gm2·Rs = 0.1 while with A_V=3 (9.5dB) it is 0.25

If Zin=Rs, the current flowing towards the circuit will be given by Vsource/2Rs. The overall voltage gain from the source to Vo is thus simply given by

$$\frac{V_O}{V_{SOURCE}} = \frac{-g_{m1} \cdot R_L \cdot R_S}{2 \cdot R_S} = \frac{-g_{m1} \cdot R_L}{2}$$

It is thus 6dB lower than the one calculated just above.

Calculating the output impedance of the circuit without Rs

To gain more insights into our circuit, let's calculate the output impedance of the stand-alone circuit without considering the input resistance Rs first. Again, one may write the two Kirchhoff equations, but now we inject Io from the output node thus on the second equation.

$$\begin{pmatrix} 0 \\ I_O \end{pmatrix} = \begin{pmatrix} g_{ms2} & -g_{m2} \\ g_{m1} & 1/R_L \end{pmatrix} \cdot \begin{pmatrix} V_{IN} \\ V_O \end{pmatrix}$$

To understand better how to find the proper signs for the various conductance of the circuit, let's consider what is happening when injecting some positive current at node Vout. If there would be no feedback to the gate of M1, the only path for the current would be through RL (assuming RL·gDSM1<<1). As the current through M1 is fixed, the only way for equilibrium to be reached is that VOUT rises so that less current flows through RL. In small signal all DC currents are kept constant, thus, to model the current reduction through RL, we add a current in the opposite direction. Hence any current flowing towards a device is by convention given the + sign.

If the resistor is connected to ground, Vout and the current would increase. If the resistor is connected to VDD the current is also entering the resistor with the same sign though actually the overall current in that device is reduced. In fact, it is the DC current that has an opposite direction in a resistor connected to VDD (-) compared to one at VSS (+). Also recall that in small signal analysis all DC supplies are to be shorted due to the superposition principle (and all current sources opened). There is thus no difference with a component connected to VDD or VSS.
Now, if Vout raises due to the current in RL, as M2 is a pure voltage follower with a gain of 1, some additional current given by gm1*dVout will be sunk by M1. It will thus partly lower Vout, but not completely, otherwise there would be no additional current flowing through M1. The output resistance is thus lowered.
Solving the above system of equation for Zo with gms2=gm (local bulk condition), our intuitive reasoning is confirmed since it is given by

$$Z_O = \frac{1}{g_{m1} + 1/R_L}$$

If gm1*RL=1, the circuit is equivalent to a resistance RL/2 with half of the injected current Iout flowing through each device. Whether the resistors are connected between VDD and VSS, or both to either VDD or VSS does not change anything from a small signal analysis.
We also note that Zo may not be higher than RL

Calculating the output impedance of the circuit with Rs included

Now let's calculate the output impedance of the circuit with Rs included. We have thus to modify the coefficient a in our matrix as well by adding 1/Rs in parallel with gms2.

$$\begin{pmatrix} 0 \\ I_O \end{pmatrix} = \begin{pmatrix} 1/R_S + g_{ms2} & -g_{m2} \\ g_{m1} & 1/R_L \end{pmatrix} \cdot \begin{pmatrix} V_{IN} \\ V_O \end{pmatrix}$$

Substituting Vin by Vo in the second equation after calculating Vin/Vo with the first one, one obtains for the circuit output admittance

$$Y_O = \frac{I_O}{V_O} = g_{m1} \cdot \frac{g_{m2}}{1/R_S + g_{ms2}} + 1/R_L$$

The output conductance is thus lowered compared to the previous case.

With M2 having a local bulk, the output impedance simplifies to

$$Z_O = \frac{1}{\frac{R_S \cdot g_{m2} \cdot g_{m1}}{1 + R_S \cdot g_{m2}} + 1/R_L}$$

As we must satisfy the input match condition, we could eliminate one parameter. gm1 expressed as a function of the other parameters from the Zin calculation is given by

$$g_{m1} = \frac{1}{R_S \cdot R_L} \cdot \frac{1}{g_{m2}} - {}^{1}/_{R_L}$$

The special case when gm1 = 0 obtained for Rs·gm2=0 is equivalent to removing M1 and having M2 providing the input matching condition alone. It is not the desired circuit operation since we have no amplification. To get a functional circuit, we must have Rs·gm2<<1

After simplification, one obtains

$$Z_O = \frac{R_L \cdot (1 + R_S \cdot g_{m2})}{2}$$

Under the condition that RS=Rin, the output impedance may thus not be lower than RL/2. This is a very different result from what was calculated without Rs. However the voltage gain for the signal derived above is not affected by this result.

Calculation of the output noise and noise factor

For this calculation we neglect the MOS 1/f noise. This is reasonable because our device will be operated at high frequency. M1 and M2 are thus characterized by their output noise (4kTγgm) with γ=1/2 and 2/3 for sub- and super-threshold operated devices. We also express the resistor noise via a current spectral density rather than its voltage spectral density. They are equivalent definitions given by

$$I_{n,2}^2 = \frac{4kT}{R} \quad V_{n,2}^2 = 4kT \cdot R$$

The first has units of A^2/Hz, the second V^2/Hz. Multiplying the first with R and dividing the second by R yield Pn=4kT. The definition are thus correct and equivalent.

It's much better to operate in the current domain since individual contributions may simply be summed as superposition applies for linear systems.

Now we should determine carefully what are the loads seen by such currents.

The noise of M2 is a current source placed between its drain and source.

$$I_{n,M2}^2 = 4kT \cdot \gamma \cdot g_{m2}$$

It sees both Rin and Rs in parallel hence Rs/2 when impedance is matched. At node Vin the voltage noise PSD of M2 is

$$V_{n,in,M2}^2 = kT \cdot \gamma \cdot g_{m2} \cdot R_S^2$$

And at the output node Vo

$$V_{n,O,M2}^2 = kT \cdot \gamma \cdot g_{m2} \cdot R_S^2 \cdot g_{m1}^2 \cdot R_L^2$$

Similarly, the voltage noise PSD contributed by Rs at the output under impedance matching condition is given by

$$V_{n,O,RS}^2 = kT \cdot R_S \cdot g_{m1}^2 \cdot R_L^2$$

The equivalent output noise current PSD contributed by M1 and RL is given by

$$I_{n,O,M1,RL}^2 = 4kT \cdot \left(\frac{1}{R_L} + \gamma \cdot g_{m1}\right)$$

It should be multiplied by the square of the output resistance calculated previously to obtain the voltage noise PSD yielding

$$V_{n,O,,M1,RL}^2 = kT \cdot \left(\frac{1}{R_L} + \gamma \cdot g_{m1}\right) \cdot R_L^2 \cdot (1 + R_S \cdot g_{m2})^2$$

The total output noise is simply the sum of the 3 contributions calculated above. The noise factor definition is the ratio of the output noise voltage PSD divided by the output noise of the source resistor. It is given by

$$F = \frac{V_{n,O,,RS}^2 + V_{n,O,,M2}^2 + V_{n,O,,M1,RL}^2}{V_{n,O,,RS}^2}$$
$$= 1 + \frac{kT \cdot \gamma \cdot g_{m2} \cdot R_S^2 \cdot g_{m1}^2 \cdot R_L^2 + kT \cdot \left(\frac{1}{R_L} + \gamma \cdot g_{m1}\right) \cdot R_L^2 \cdot (1 + R_S \cdot g_{m2})^2}{kT \cdot R_S \cdot g_{m1}^2 \cdot R_L^2}$$

After simplification, one gets,

$$F = 1 + \gamma \cdot g_{m2} \cdot R_S + \left(\frac{1}{R_L} + \gamma \cdot g_{m1}\right) \cdot \frac{(1 + R_S \cdot g_{m2})^2}{R_S \cdot g_{m1}^2}$$

This is what we would have obtained as well when computing the NF at node VIN (the output noise of M2 and RL having been divided by the square of the voltage gain $Rs^2 \cdot gm1^2$).

To help us design the circuit let's rewrite the Zin=Rs equation linking the gain, A_V to the gm2·Rs product and the output impedance one. Setting RS=50Ω, we can compute gm2 as a function of the desired voltage gain. This imposes the gm1·RL product as well but not their values which will be determined by the noise figure.

$$\frac{1}{(1 + A_V)} = g_{m2} \cdot R_S$$

$$A_V = \frac{1}{g_{m2} \cdot R_S} - 1$$

We may thus reformulate the noise factor as

$$F = 1 + \gamma \cdot \frac{1}{(1 + A_V)} + (1 + \gamma \cdot A_V) \cdot \frac{R_L}{R_S} \cdot \frac{1}{A_V^2} \cdot \left(\frac{2 + A_V}{1 + A_V}\right)^2 \approx 1 + \frac{\gamma}{A_V} \cdot \left(1 + \frac{R_L}{R_S}\right)$$

The second term above before the simplification is the contribution of M2 to the noise factor. It is divided by the voltage gain which is the ratio of Vout/Vin hence the voltages that are applied to the gate and source of M2 respectively. When loaded with Rs, the voltage follower operates indeed as an attenuator with an attenuation equal to A_V (using the same definition as for filters). In different words, the equivalent noise resistance 1/γgm2 is much bigger than Rs hence the parallel combination of Rs and is close to Rs and the noise dominated by Rs.

The third term, $RL \cdot (1+\gamma A_V)$, denotes respectively the contribution of RL and M1. Consequently, M1 is significantly noisier than RL. Consider again two resistors in parallel, RL and 1/γgm1, but now RL is much bigger thus M1 contribution is the most important. Finally, after simplification, one could compare M1 and M2 contributions whose ratio is simply given by RL/Rs.

Interestingly, the circuit power gain from the antenna to the output is given by $1/4 \cdot A_V^2 \cdot Rs/Ro$. The output impedance can be rewritten as a function of the voltage gain as

$$Z_O = \frac{R_L \cdot (1 + R_S \cdot g_{m2})}{2} = \frac{R_L}{2} \cdot \frac{(2 + A_V)}{(1 + A_V)}$$

It is thus close to RL/2.

Note however that this circuit is not designed to drive a matched load having an input impedance of RL/2 as the output is not a voltage source but rather a current one. This problem could be solved by loading the output stage with an inductor with a high output equivalent resistance Rp and RL/2 implemented by the input resistance of the next circuit after AC-coupling. With Rp>>RL/2, the circuit would behave as expected without noise degradation.